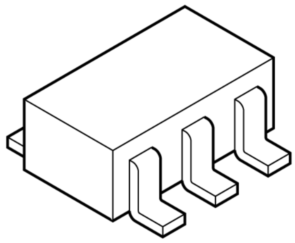
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S54F,TC75S54FU,TC75S54FE

Single Operational Amplifier

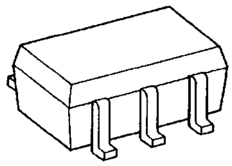
The TC75S54F/TC75S54FU/TC75S54FE is a CMOS single-operation amplifier which incorporates a phase compensation circuit. It is designed for use with a low-voltage, low-current power supply; this differentiates this device from conventional general-purpose bipolar op-amps.

TC75S54F



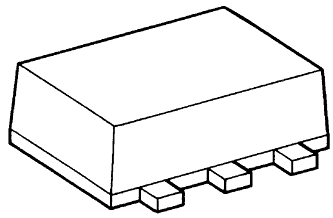
SSOP5-P-0.95

TC75S54FU



SSOP5-P-0.65A

TC75S54FE



SON5-P-0.50

Weight
SSOP5-P-0.95 : 0.014 g (typ.)
SSOP5-P-0.65A : 0.006 g (typ.)
SON5-P-0.50 : 0.003 g (typ.)

Features

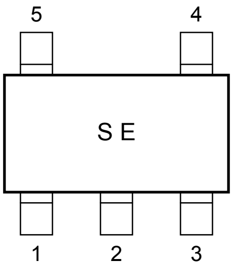
- Low-voltage operation : V_{DD} = ±0.9~3.5 V or 1.8~7 V
- Low-current power supply : I_{DD} (V_{DD} = 3 V) = 100 μA (typ.)
- Built-in phase-compensated op-amp, obviating the need for any external device
- Ultra-compact package

Absolute Maximum Ratings (Ta = 25°C)

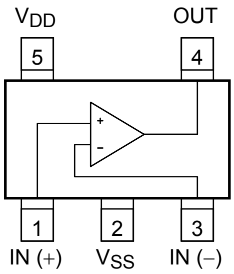
Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}, V_{SS}	7	V
Differential input voltage		DV_{IN}	±7	V
Input voltage		V_{IN}	V_{DD}~V_{SS}	V
Power dissipation	TC75S54F/FU	P_D	200	mW
	TC75S54FE		100	
Operating temperature		T_{opr}	−40~85	°C
Storage temperature		T_{stg}	−55~125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Marking (top view)



Pin Connection (top view)



Electrical Characteristics

DC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 1 kΩ	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.0	—	2.1	V
Voltage gain(open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	R_L ≧ 100 kΩ	2.9	—	—	V
	V_{OL}	4	R_L ≧ 100 kΩ	—	—	0.1	
Common mode input signal rejection ratio	CMRR	2	V_{IN} = 0.0~2.1 V	60	70	—	dB
Supply voltage rejection ratio	SVRR	1	V_{DD} = 1.8~7.0 V	60	70	—	dB
Supply current	I_{DD}	5	—	—	100	200	μA
Source current	I_{source}	6	—	100	200	—	μA
Sink current	I_{sink}	7	—	200	700	—	μA

DC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 10 kΩ	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.2	—	0.9	V
Voltage gain (open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	R_L ≧ 100 kΩ	1.7	—	—	V
	V_{OL}	4	R_L ≧ 100 kΩ	—	—	0.1	
Supply current	I_{DD}	5	—	—	80	160	μA
Source current	I_{source}	6	—	80	160	—	μA
Sink current	I_{sink}	7	—	200	600	—	μA

AC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

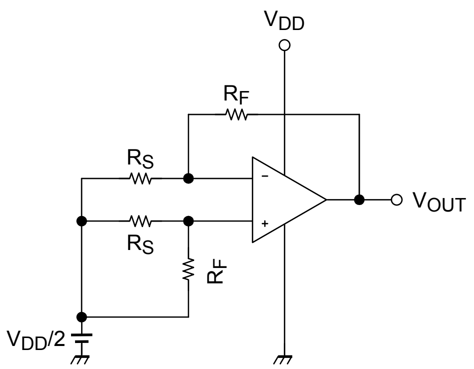
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	0.7	—	V/μs
Unity gain cross frequency	f_T	—	—	—	0.9	—	MHz

AC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	0.6	—	V/μs
Unity gain cross frequency	f_T	—	—	—	0.8	—	MHz

Test Circuit

1. SVRR, V_{IO}



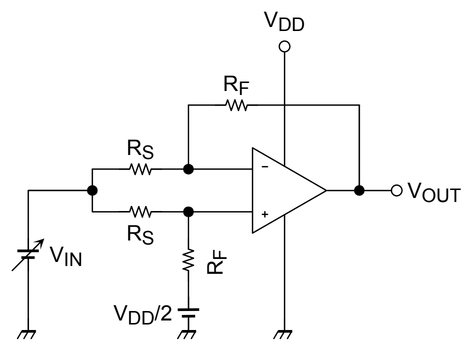
- SVRR
  For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.
  When V_{DD} = 1.8 V, $V_{DD} = V_{DD}1$ and $V_{OUT} = V_{OUT}1$
  When V_{DD} = 7.0 V, $V_{DD} = V_{DD}2$ and $V_{OUT} = V_{OUT}2$

$$SVRR = 20\,\ell og\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{DD}1 - V_{DD}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- V_{IO}
  Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMV_{IN}

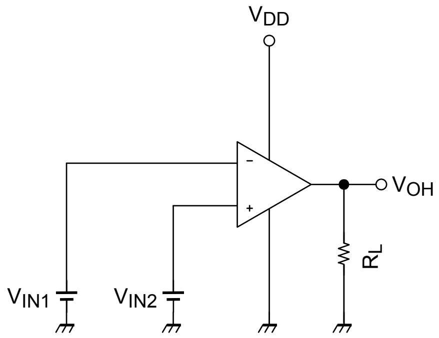


- CMRR
  Measure the V_{OUT} value, as indicated below, and calculate the value of the CMRR using the equation shown.
  When V_{IN} = 0.0 V, $V_{IN} = V_{IN}1$ and $V_{OUT} = V_{OUT}1$
  When V_{IN} = 2.1 V, $V_{IN} = V_{IN}2$ and $V_{OUT} = V_{OUT}2$

$$CMRR = 20\,\ell og\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{IN}1 - V_{IN}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- CMV_{IN}
  Input range within which the CMRR specification guarantees V_{OUT} value (as varied by the V_{IN} value).

3. V_{OH}

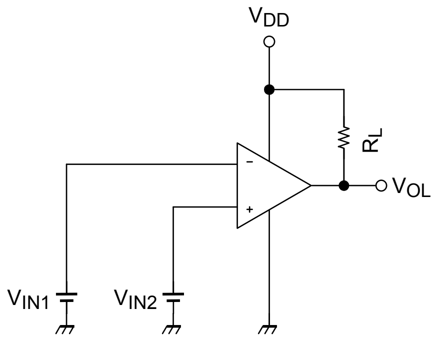


- V_{OH}

$$V_{IN1} = \frac{V_{DD}}{2} - 0.05\ \text{V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.05\ \text{V}$$

4. V_{OL}

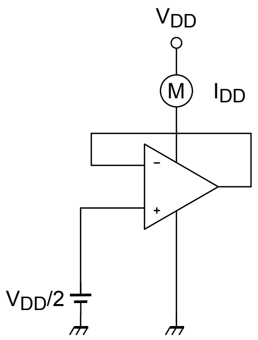


- V_{OL}

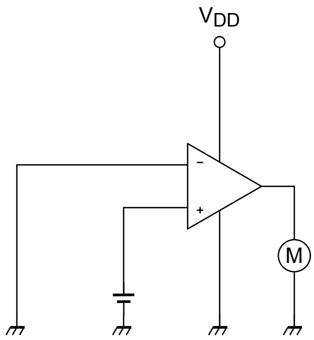
$$V_{IN1} = \frac{V_{DD}}{2} + 0.05\ \text{V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.05\ \text{V}$$

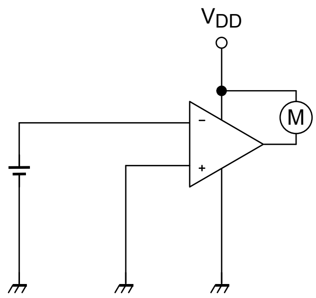
5. I_{DD}

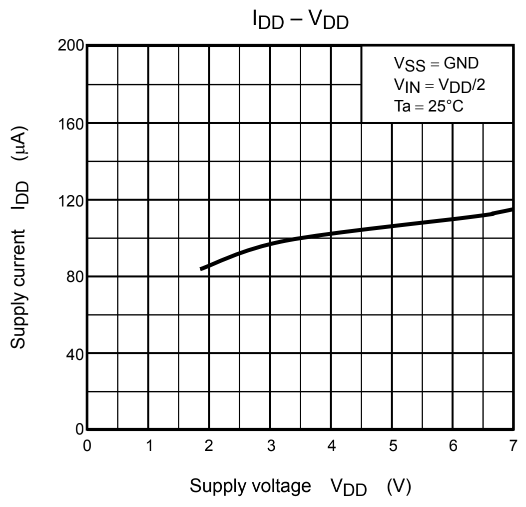


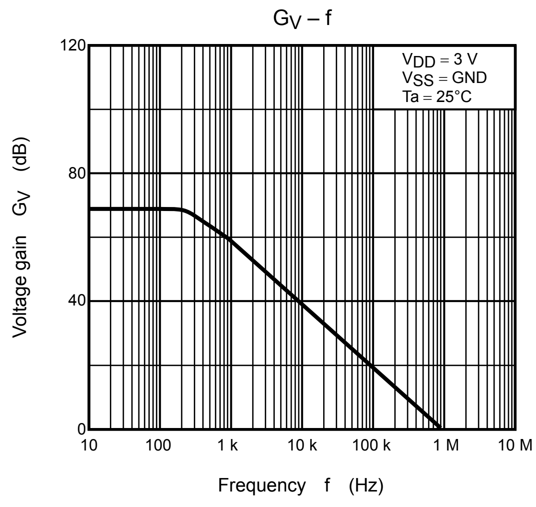
6. I_{source}

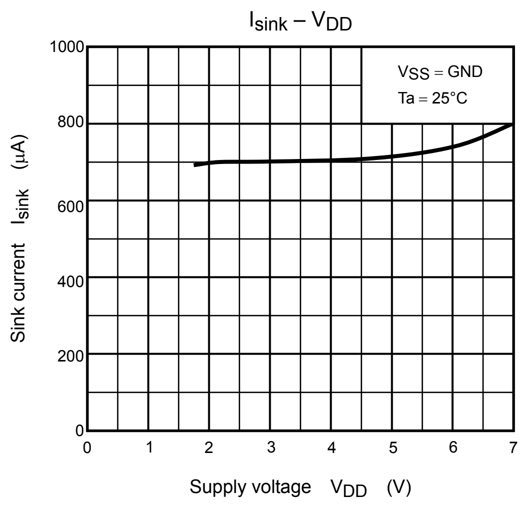


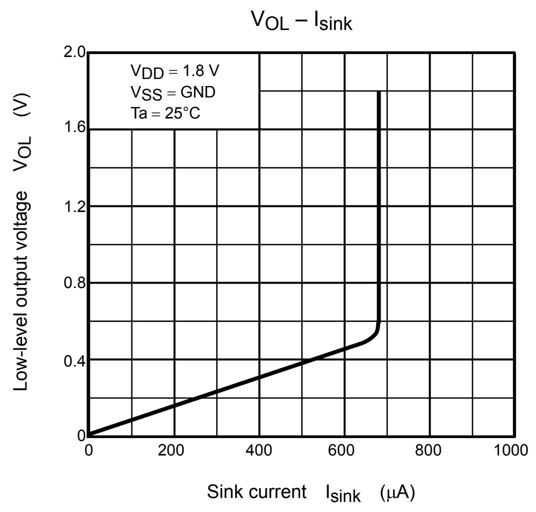
7. I_{sink}

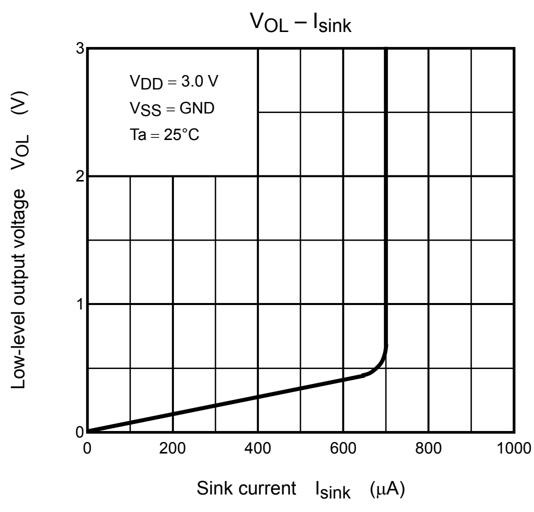


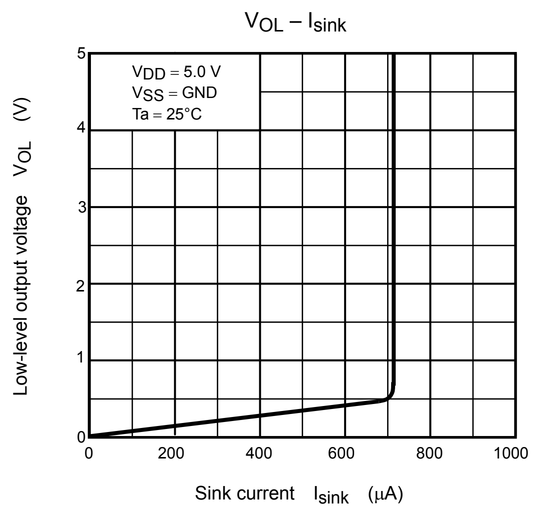

IDD – VDD
VSS = GND
VIN = VDD/2
Ta = 25°C
Supply current IDD (μA)
Supply voltage VDD (V)
0
40
80
120
160
200
0
1
2
3
4
5
6
7

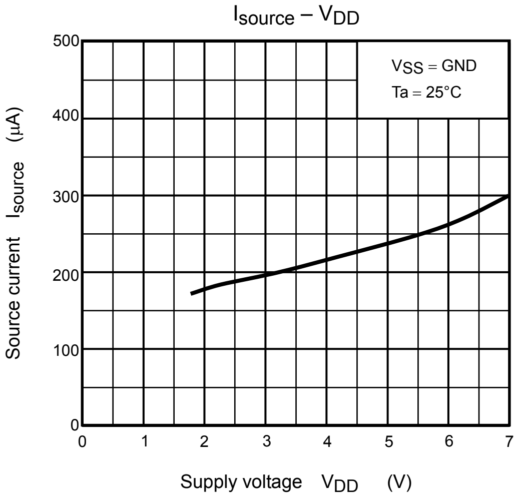

GV – f
VDD = 3 V
VSS = GND
Ta = 25°C
Voltage gain GV (dB)
Frequency f (Hz)
0
40
80
120
10
100
1 k
10 k
100 k
1 M
10 M

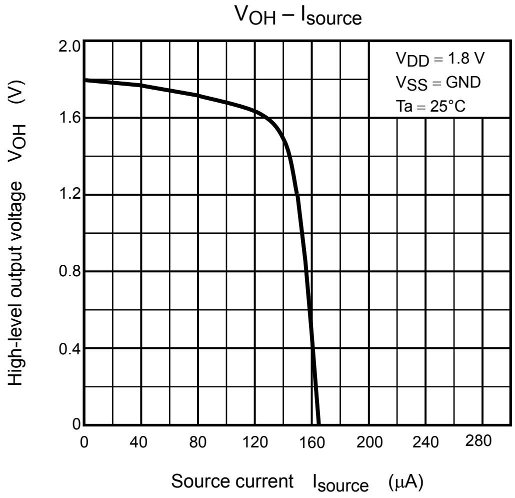

Isink – VDD
VSS = GND
Ta = 25°C
Sink current Isink (μA)
Supply voltage VDD (V)
0
200
400
600
800
1000
0
1
2
3
4
5
6
7

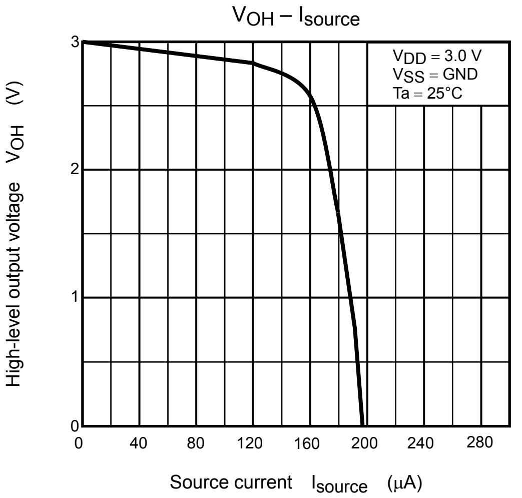

VOL – Isink
VDD = 1.8 V
VSS = GND
Ta = 25°C
Low-level output voltage VOL (V)
Sink current Isink (μA)
0
0.4
0.8
1.2
1.6
2.0
0
200
400
600
800
1000

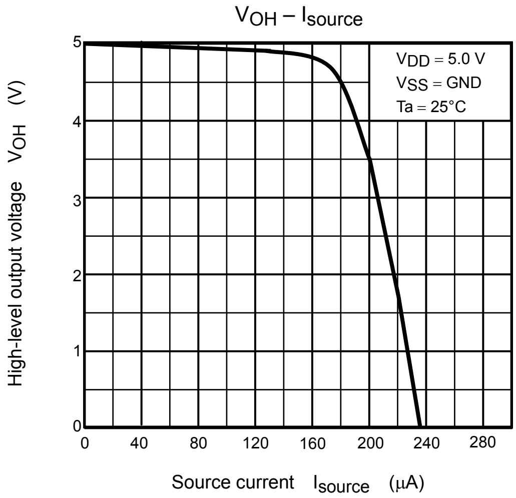

VOL – Isink
VDD = 3.0 V
VSS = GND
Ta = 25°C
Low-level output voltage VOL (V)
Sink current Isink (μA)
0
1
2
3
0
200
400
600
800
1000

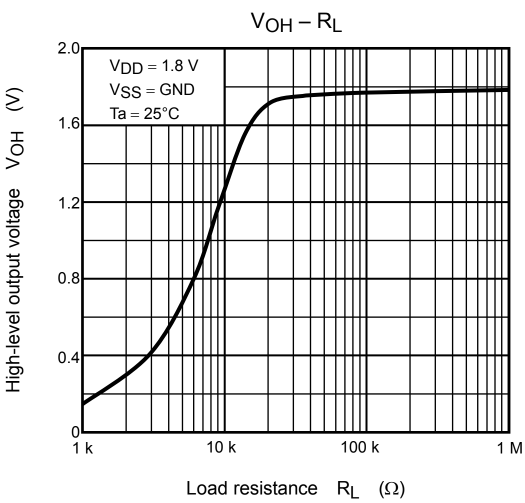

VOL – Isink
VDD = 5.0 V
VSS = GND
Ta = 25°C
Low-level output voltage VOL (V)
Sink current Isink (μA)
0
1
2
3
4
5
0
200
400
600
800
1000

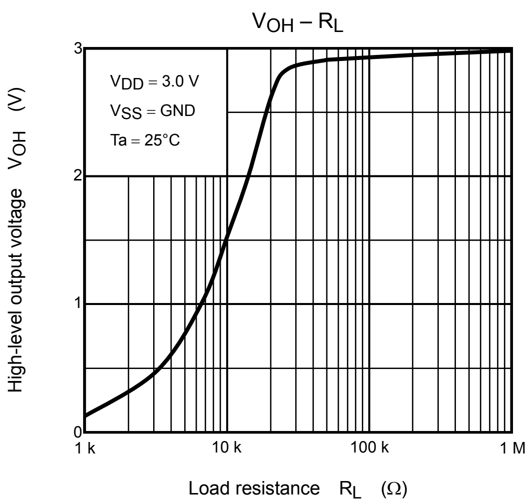

I_{source} – V_{DD}
V_{SS} = GND
Ta = 25°C
Source current I_{source} (μA)
Supply voltage V_{DD} (V)
0
100
200
300
400
500
0 1 2 3 4 5 6 7

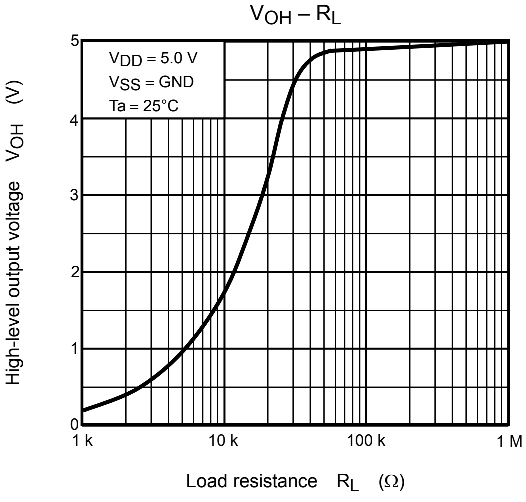

V_{OH} – I_{source}
V_{DD} = 1.8 V
V_{SS} = GND
Ta = 25°C
High-level output voltage V_{OH} (V)
Source current I_{source} (μA)
0
0.4
0.8
1.2
1.6
2.0
0 40 80 120 160 200 240 280


V_{OH} – I_{source}
V_{DD} = 3.0 V
V_{SS} = GND
Ta = 25°C
High-level output voltage V_{OH} (V)
Source current I_{source} (μA)
0
1
2
3
0 40 80 120 160 200 240 280

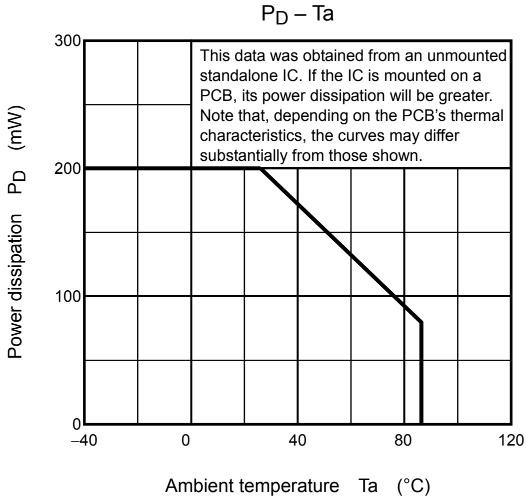

V_{OH} – I_{source}
V_{DD} = 5.0 V
V_{SS} = GND
Ta = 25°C
High-level output voltage V_{OH} (V)
Source current I_{source} (μA)
0
1
2
3
4
5
0 40 80 120 160 200 240 280


V_{OH} – R_L
V_{DD} = 1.8 V
V_{SS} = GND
Ta = 25°C
High-level output voltage V_{OH} (V)
Load resistance R_L (Ω)
0
0.4
0.8
1.2
1.6
2.0
1 k 10 k 100 k 1 M


V_{OH} – R_L
V_{DD} = 3.0 V
V_{SS} = GND
Ta = 25°C
High-level output voltage V_{OH} (V)
Load resistance R_L (Ω)
0
1
2
3
1 k 10 k 100 k 1 M

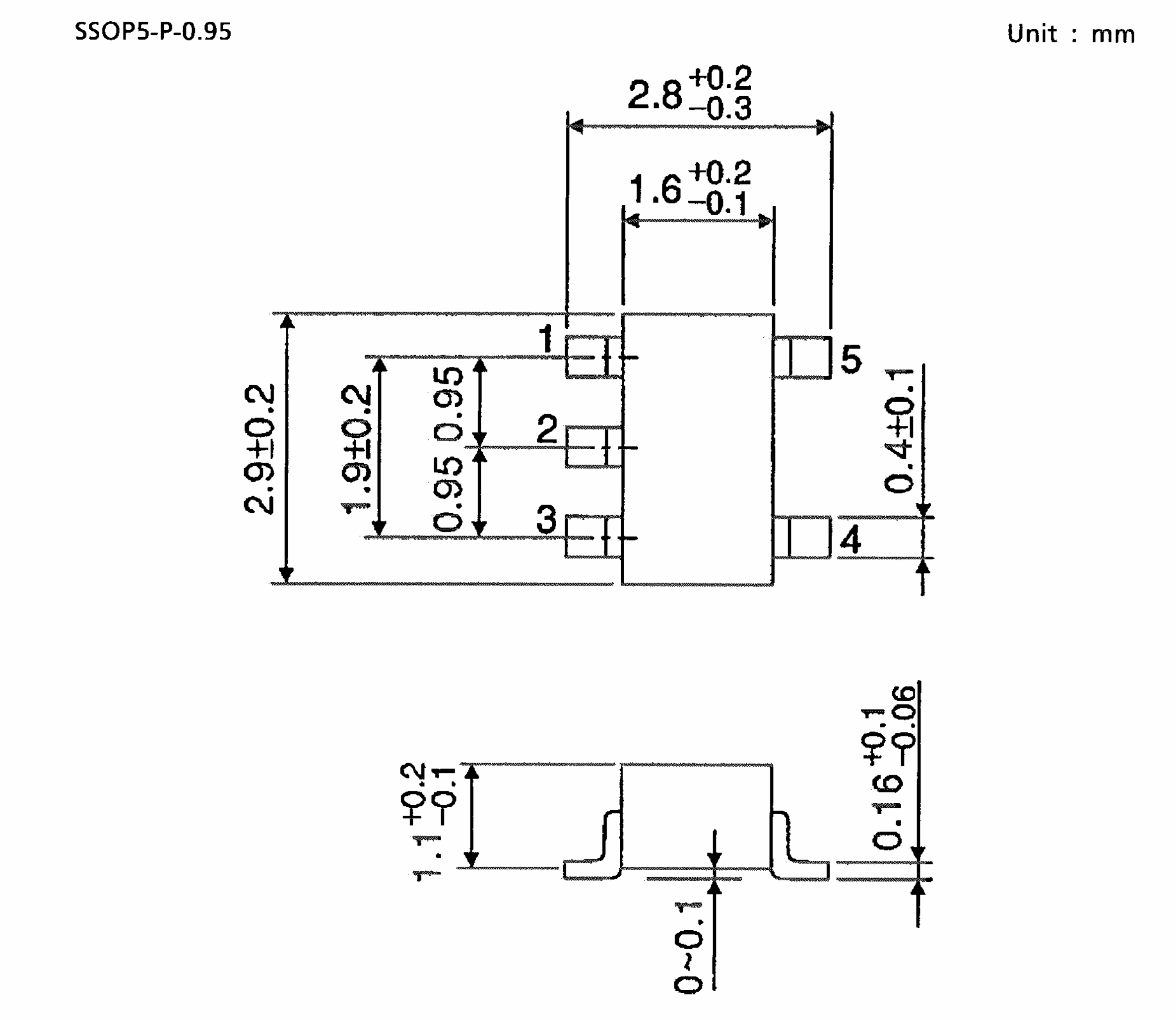


V_{OH} – R_L
V_{DD} = 5.0 V
V_{SS} = GND
Ta = 25°C
High-level output voltage V_{OH} (V)
0
1
2
3
4
5
1 k
10 k
100 k
1 M
Load resistance R_L (Ω)



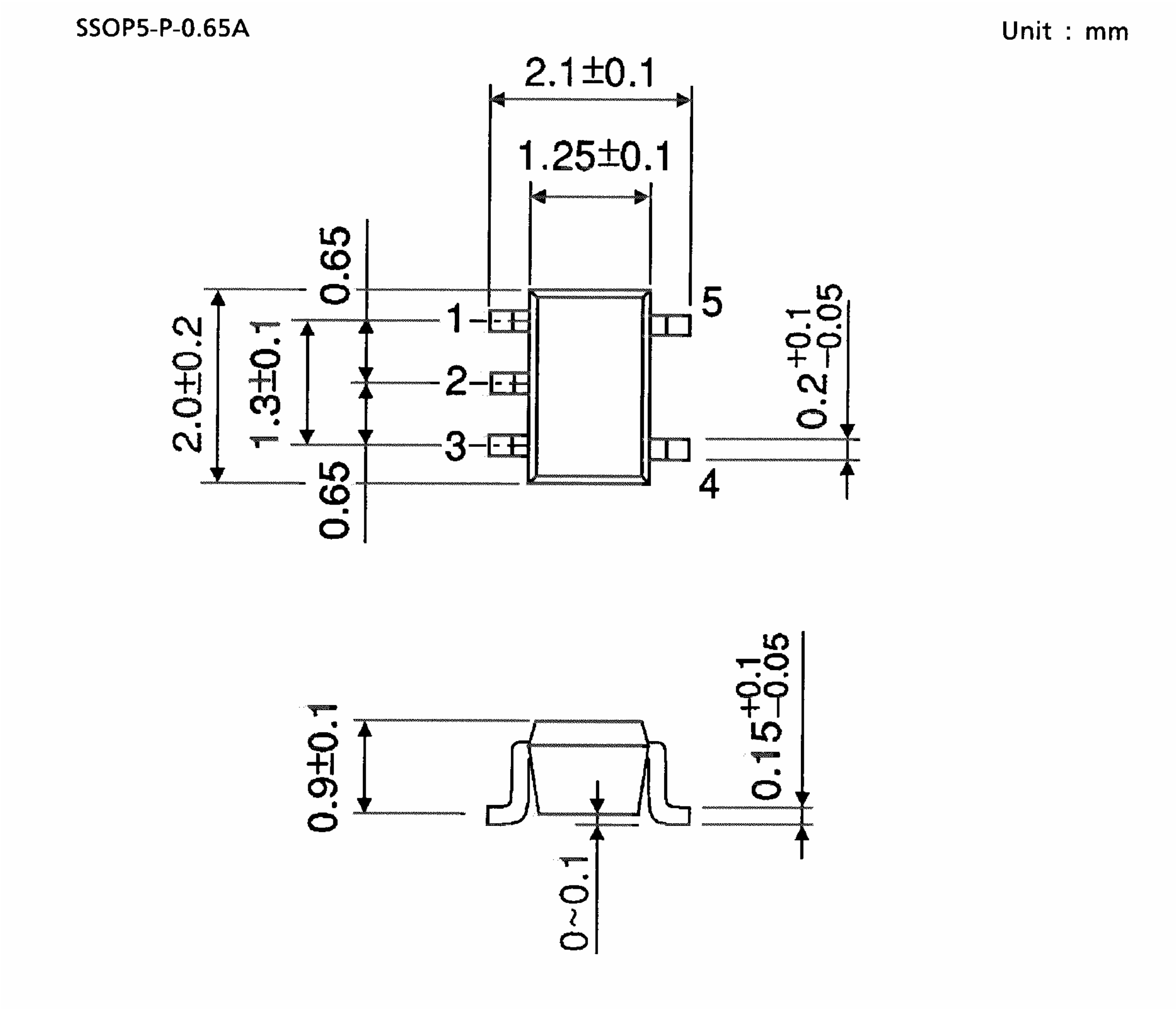
P_D – Ta
This data was obtained from an unmounted standalone IC. If the IC is mounted on a PCB, its power dissipation will be greater. Note that, depending on the PCB's thermal characteristics, the curves may differ substantially from those shown.
Power dissipation P_D (mW)
0
100
200
300
–40
0
40
80
120
Ambient temperature Ta (°C)

Package Dimensions



Weight: 0.014 g (typ.)

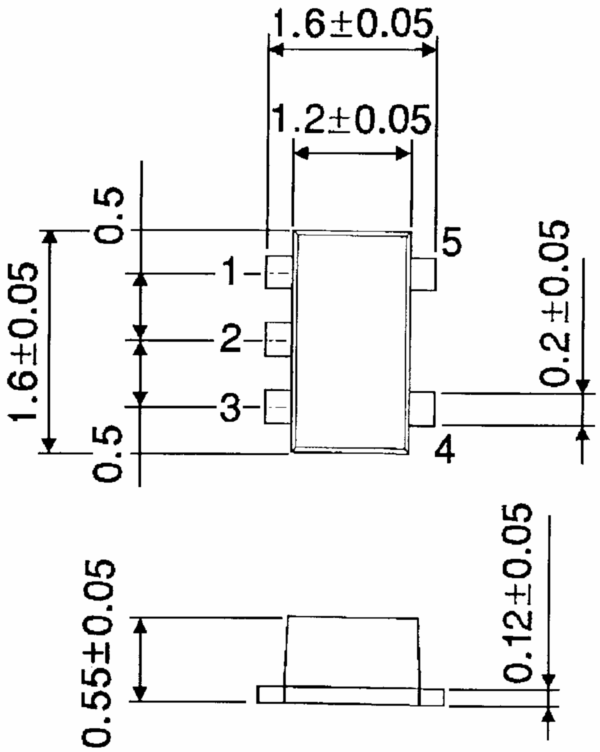
Package Dimensions



Weight: 0.006 g (typ.)

Package Dimensions

SON5-P-0.50 Unit : mm



Weight: 0.003 g (typ.)

RESTRICTIONS ON PRODUCT USE